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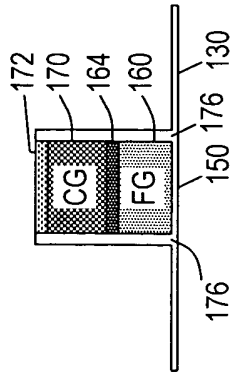


FIG. 1
PRIOR ART

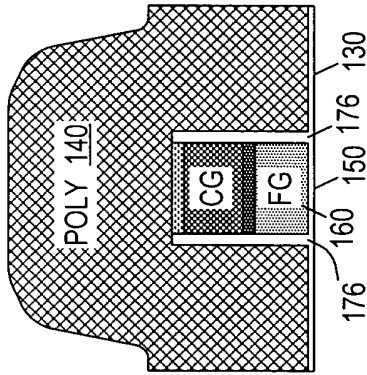


FIG. 2
PRIOR ART

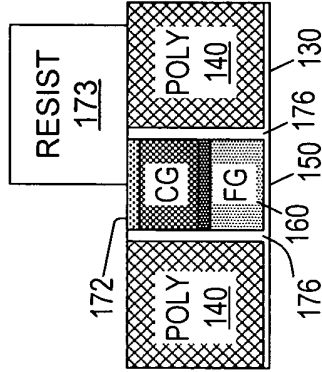


FIG. 3
PRIOR ART

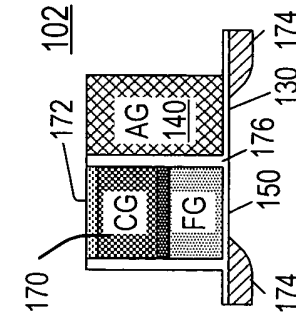


FIG. 4
PRIOR ART

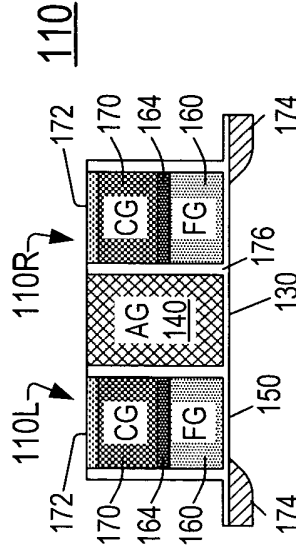
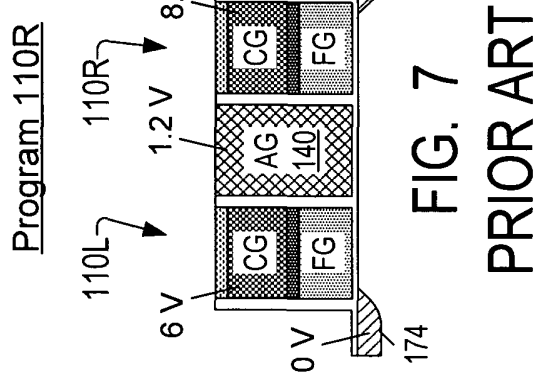
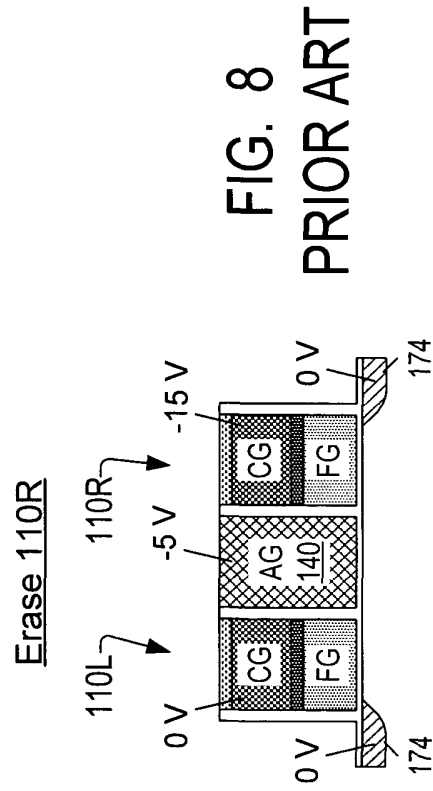
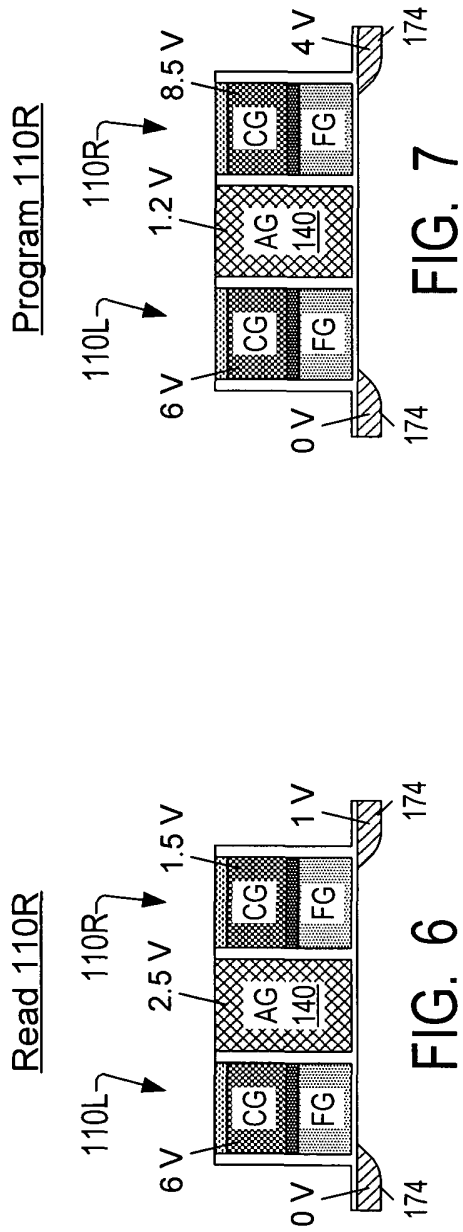


FIG. 5
PRIOR ART

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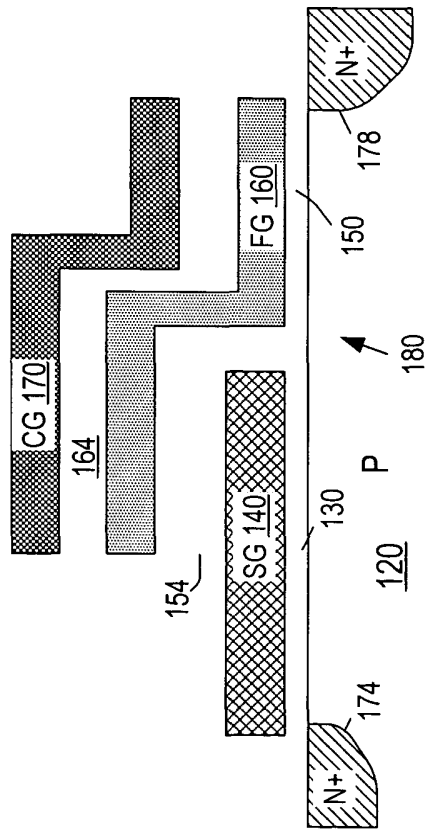
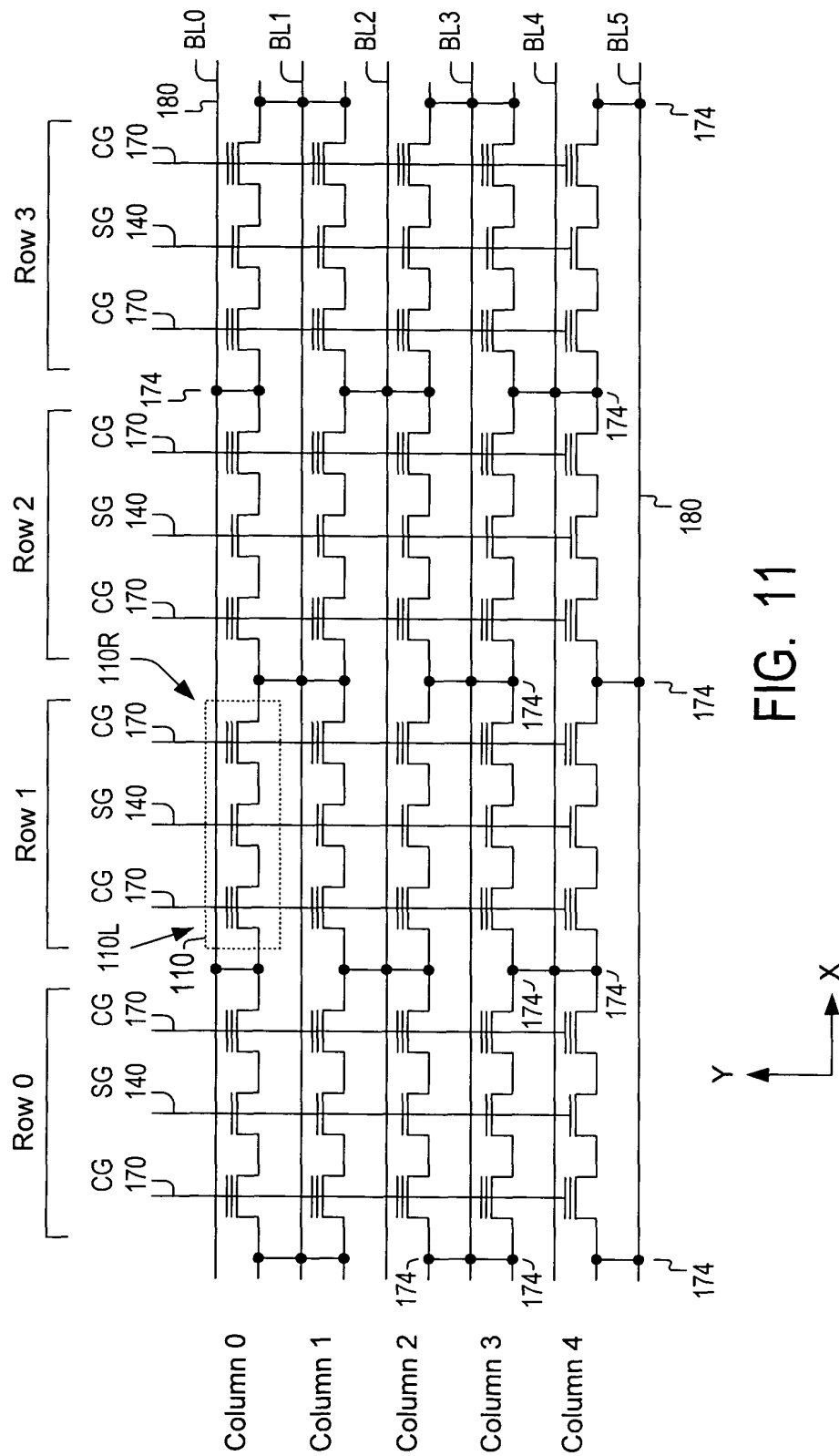
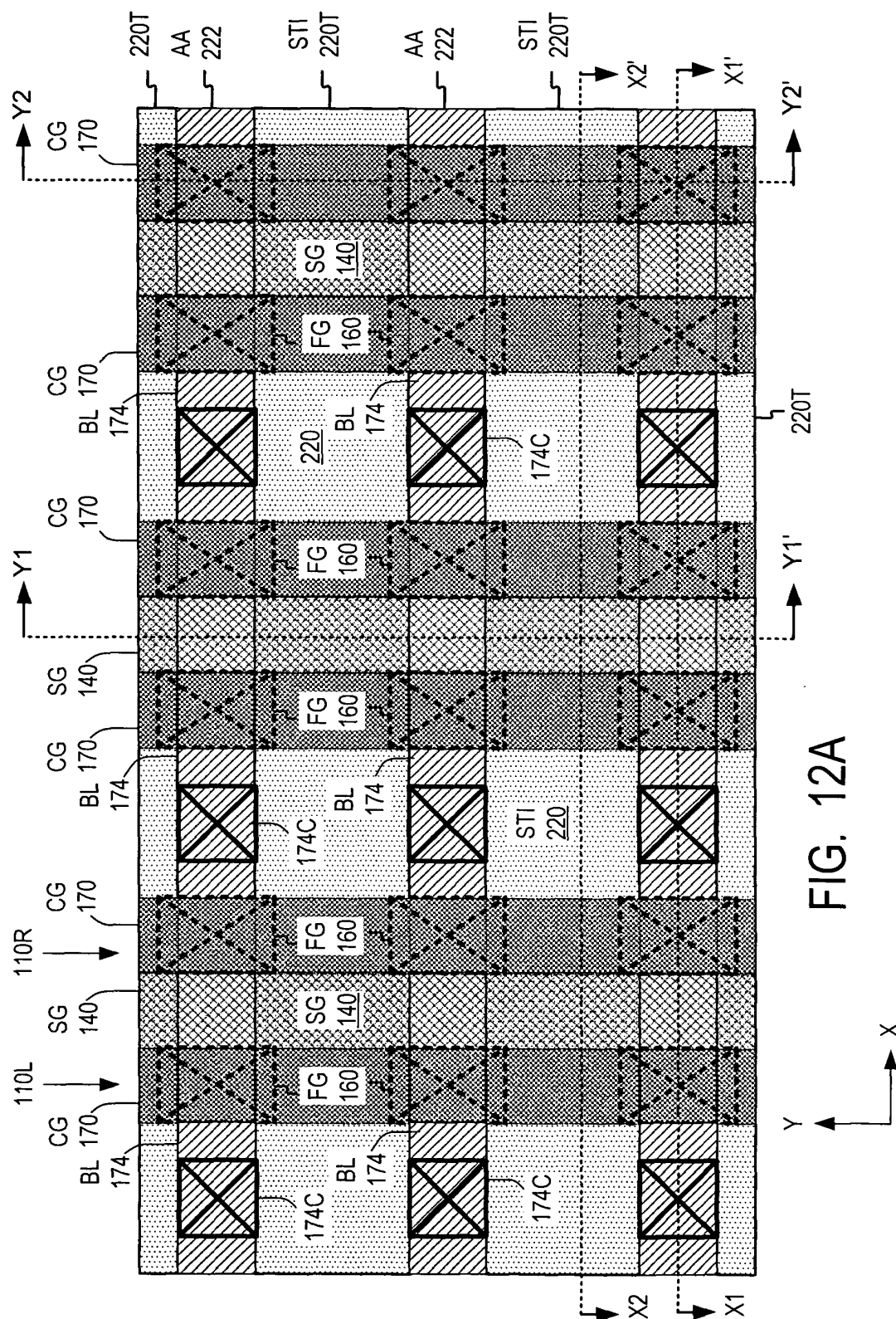


FIG. 9
PRIOR ART

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FIG. 12B

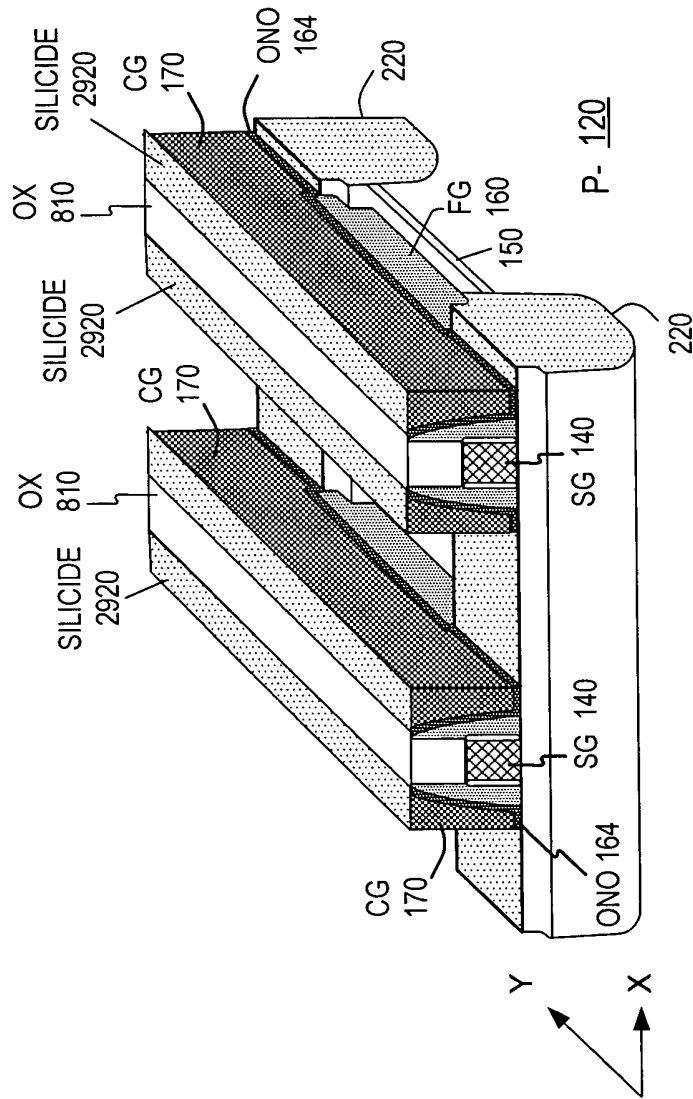


FIG. 13 (Y1-Y1')

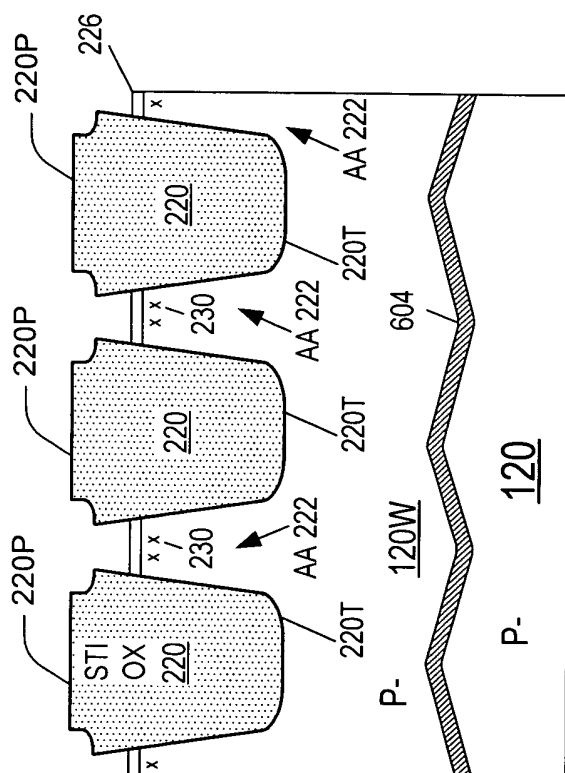


FIG. 14B
(PERIPHERY)

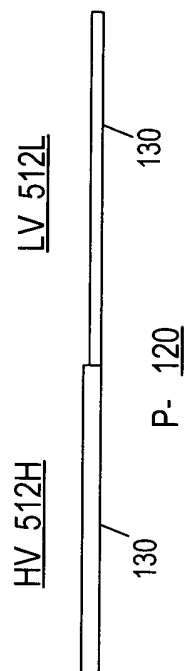
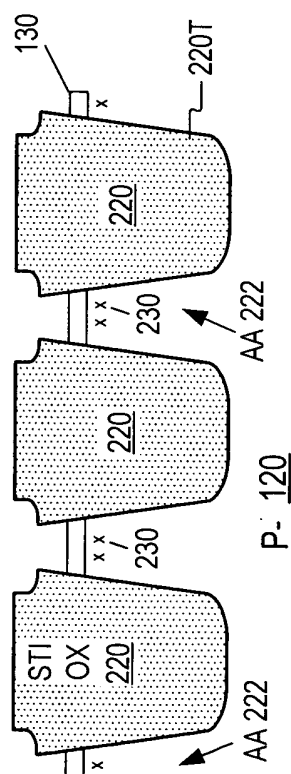


FIG. 14A (Y1-Y1')



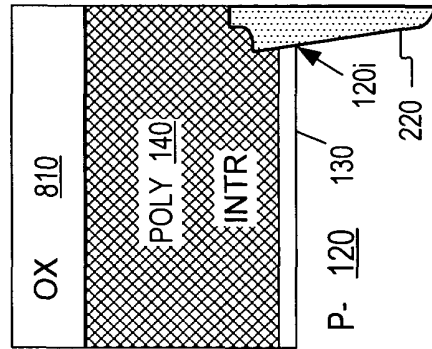


FIG. 15B
(PERIPHERY)

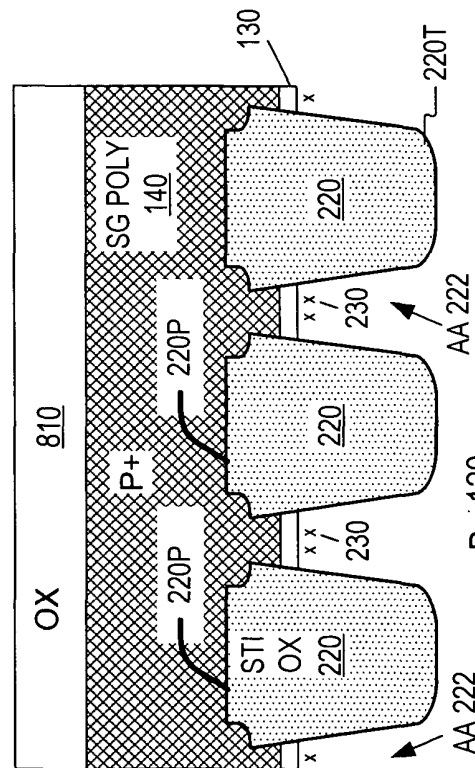


FIG. 15A (Y1-Y1')

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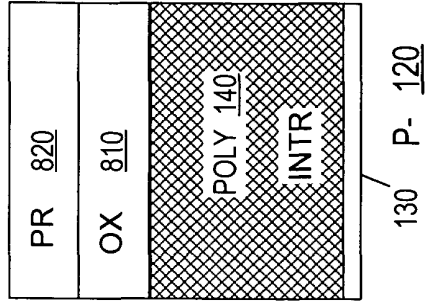


FIG. 16B
(PERIPHERY)

FIG. 17

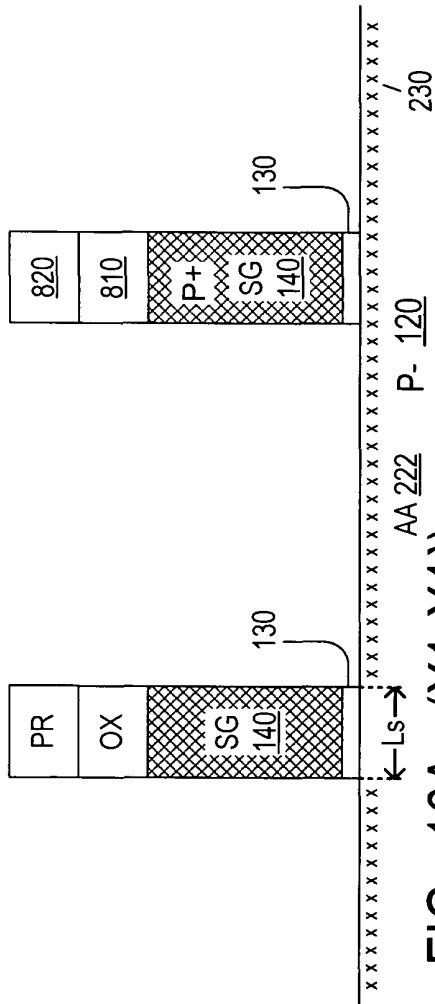


FIG. 16A (X1-X1')

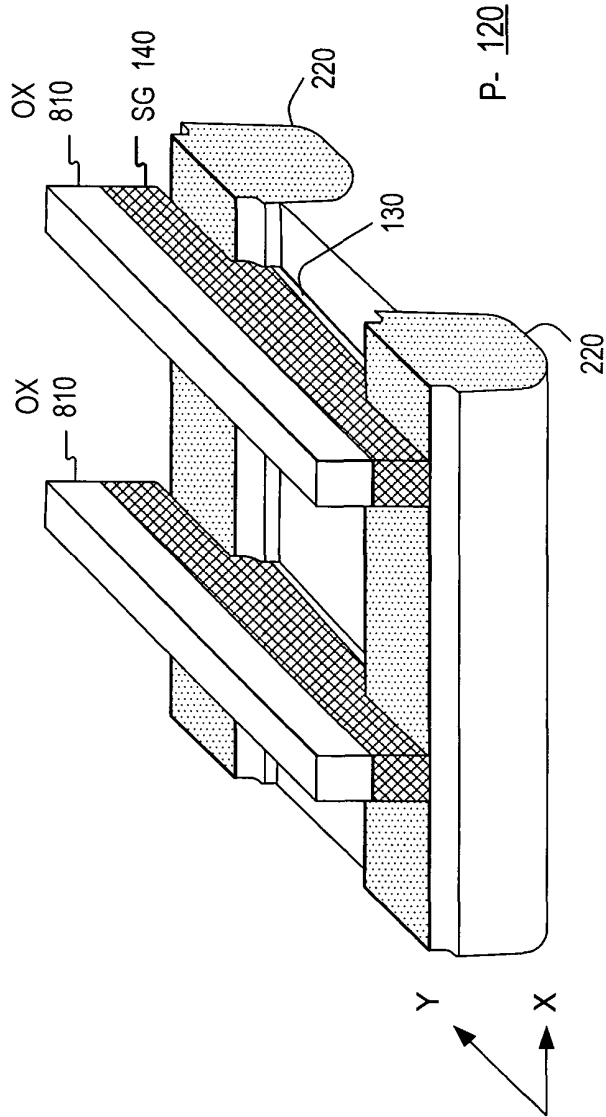


FIG. 18
(X1-X1')

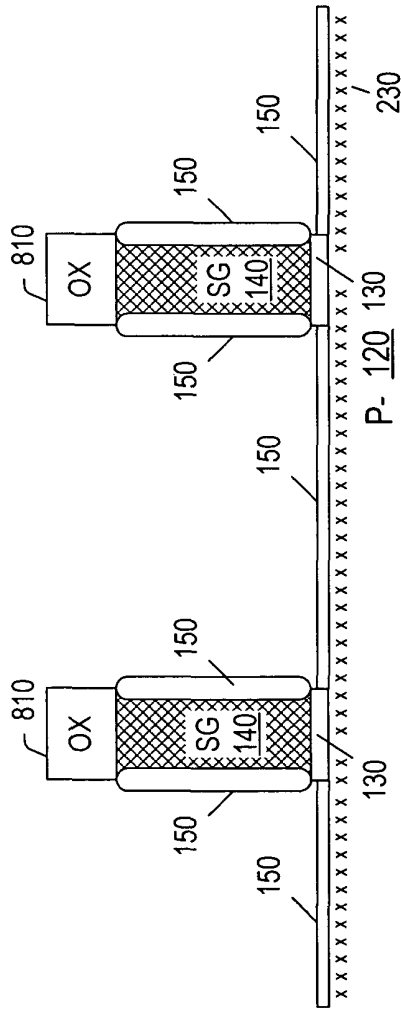


FIG. 19A (X1-X1')

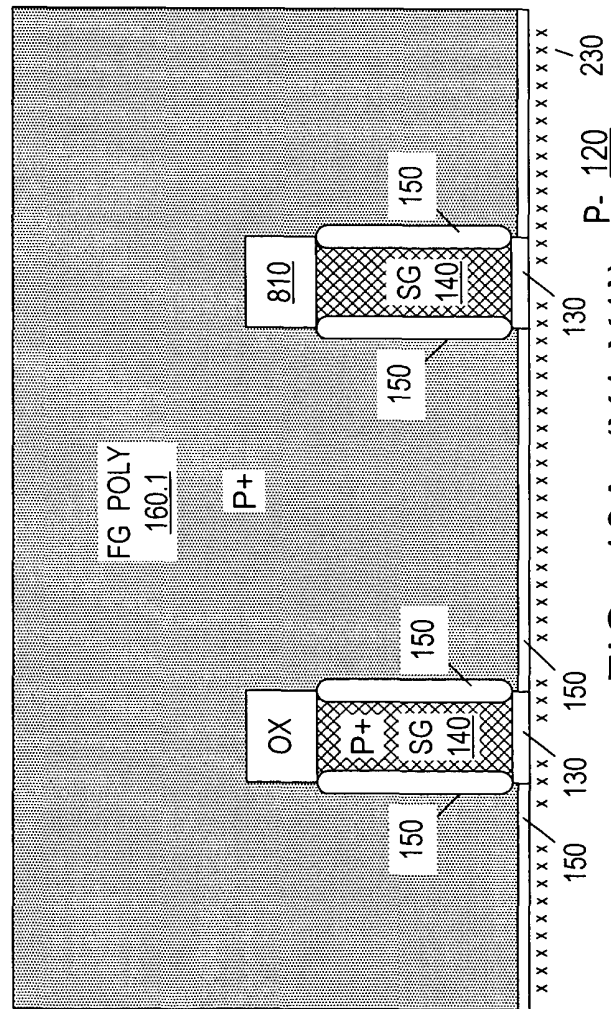
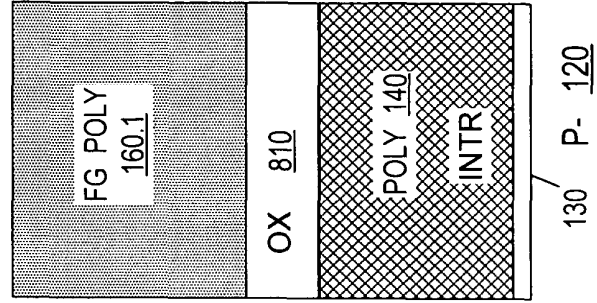


FIG. 19B (PERIPHERY)



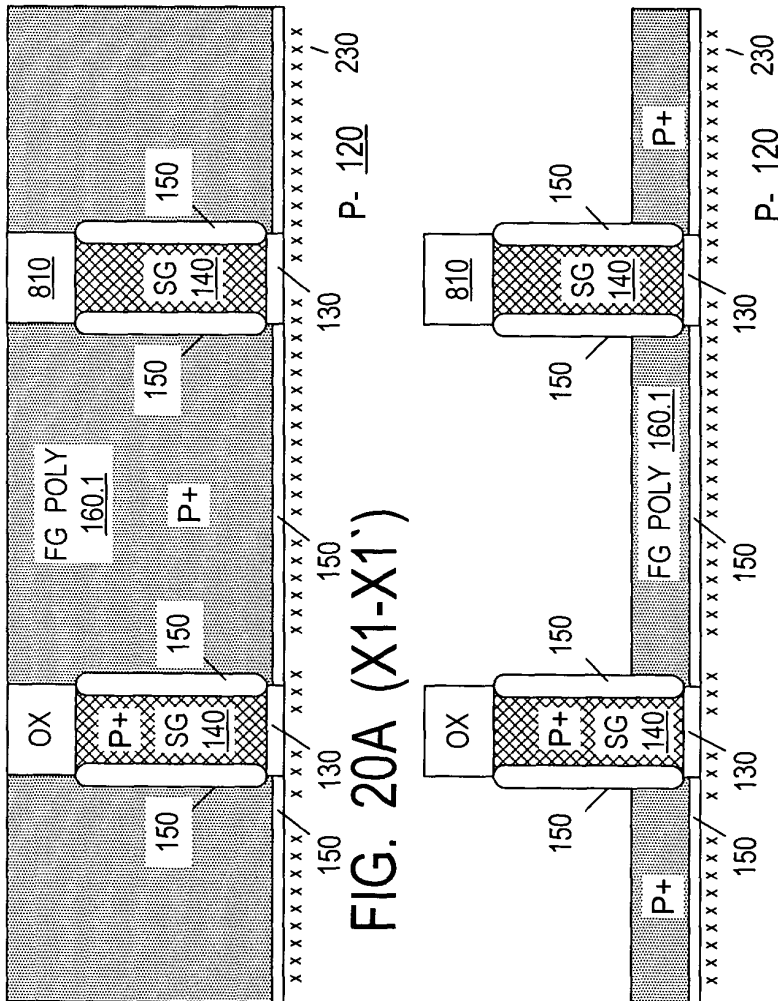


FIG. 20A (X1-X1')

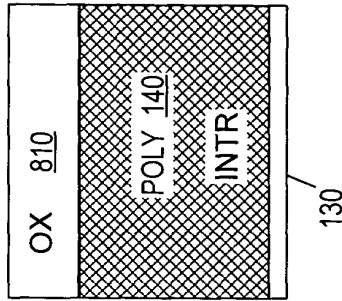


FIG. 20B (PERIPHERY)

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FIG. 21A
(X1-X1')

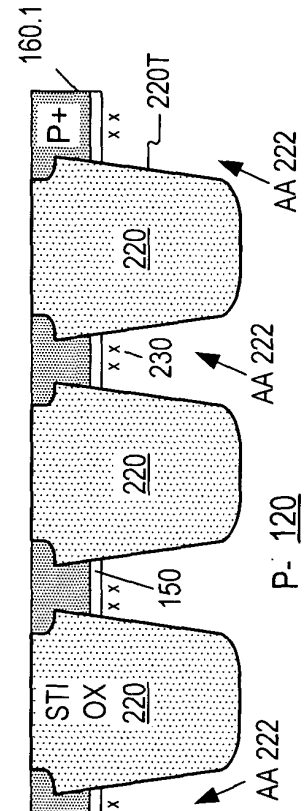
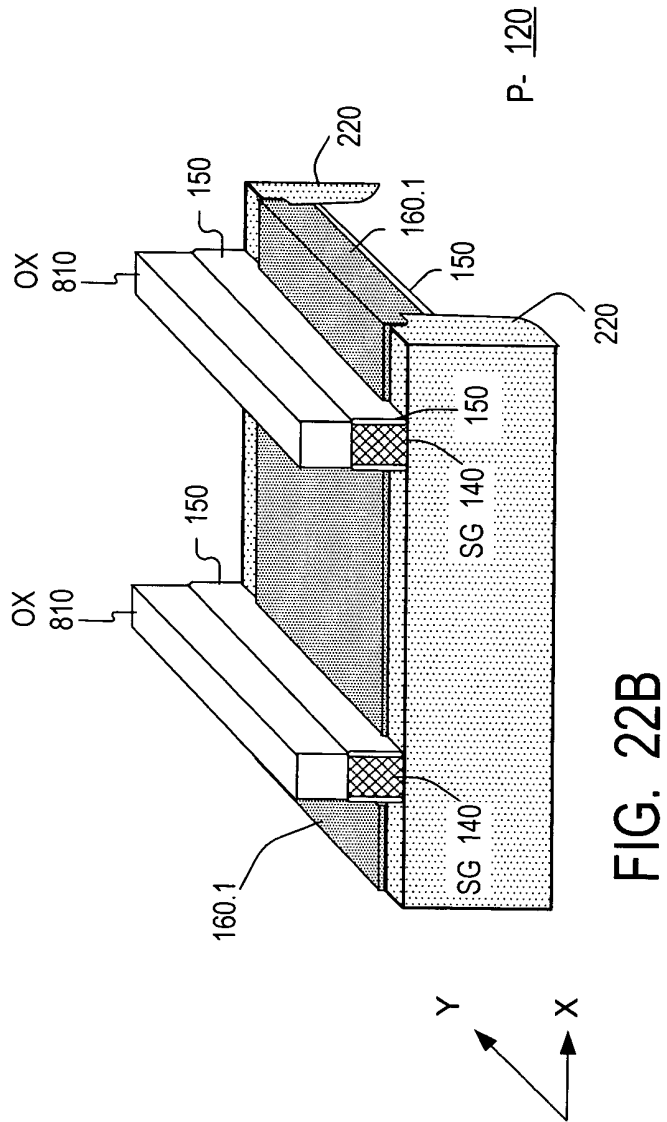
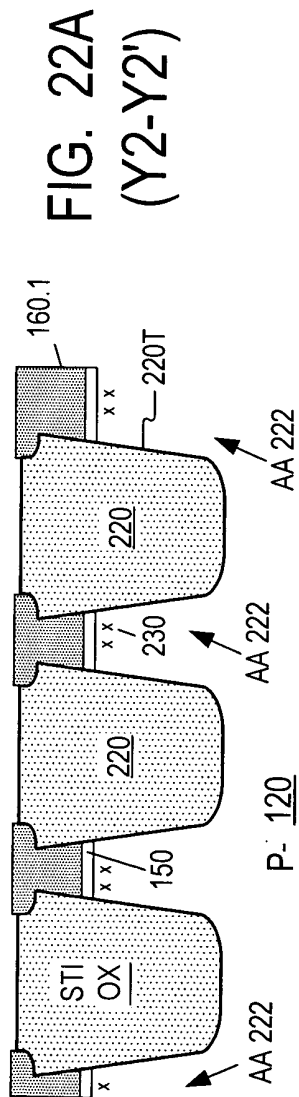


FIG. 21B
(Y2-Y2')

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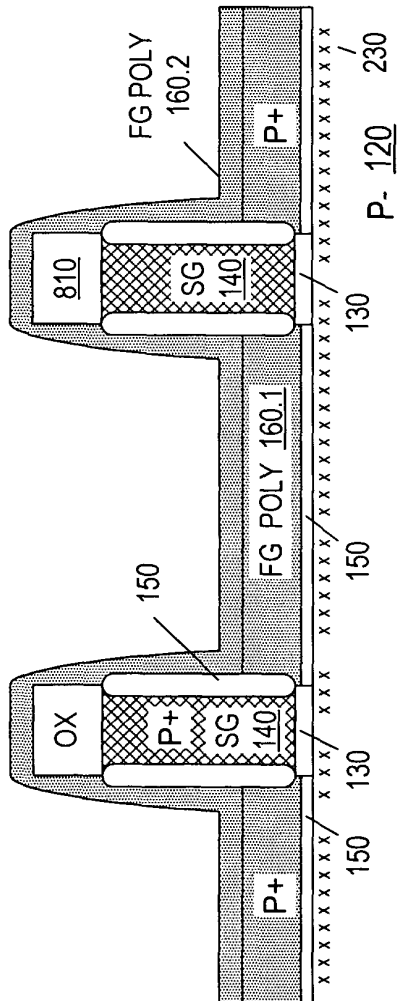


FIG. 23A (X1-X1'')

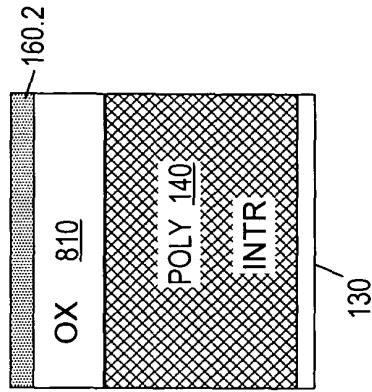


FIG. 23B (PERIPHERY)

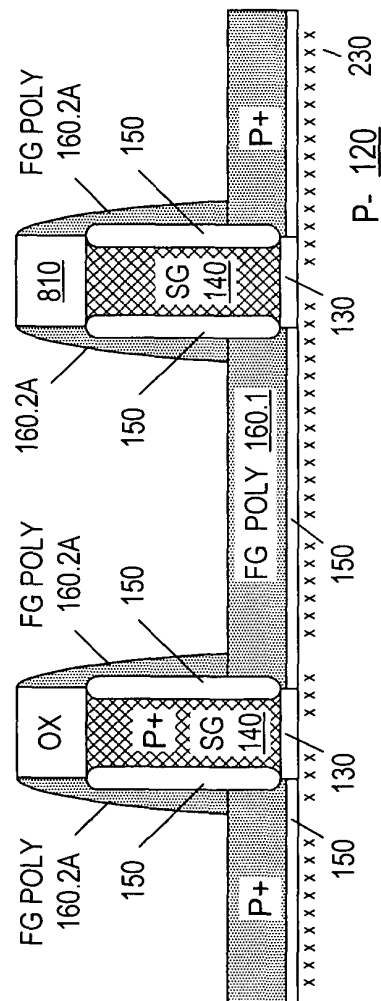


FIG. 24A (X1-X1'')

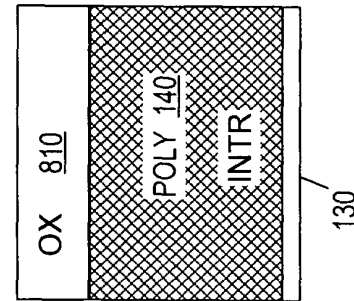


FIG. 24B (PERIPHERY)

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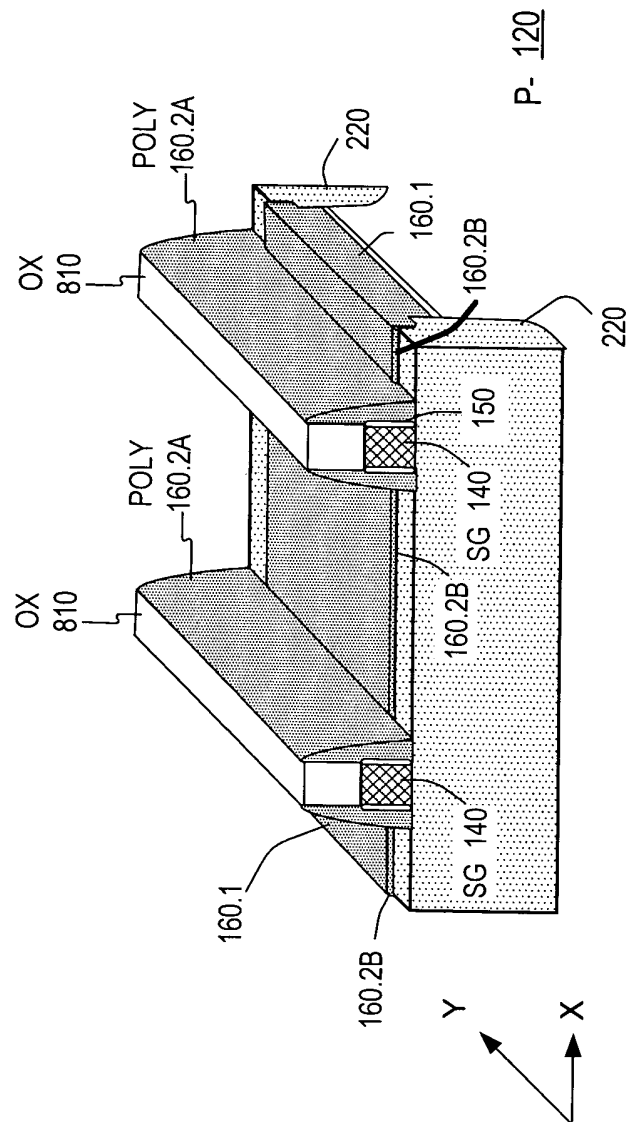


FIG. 24C

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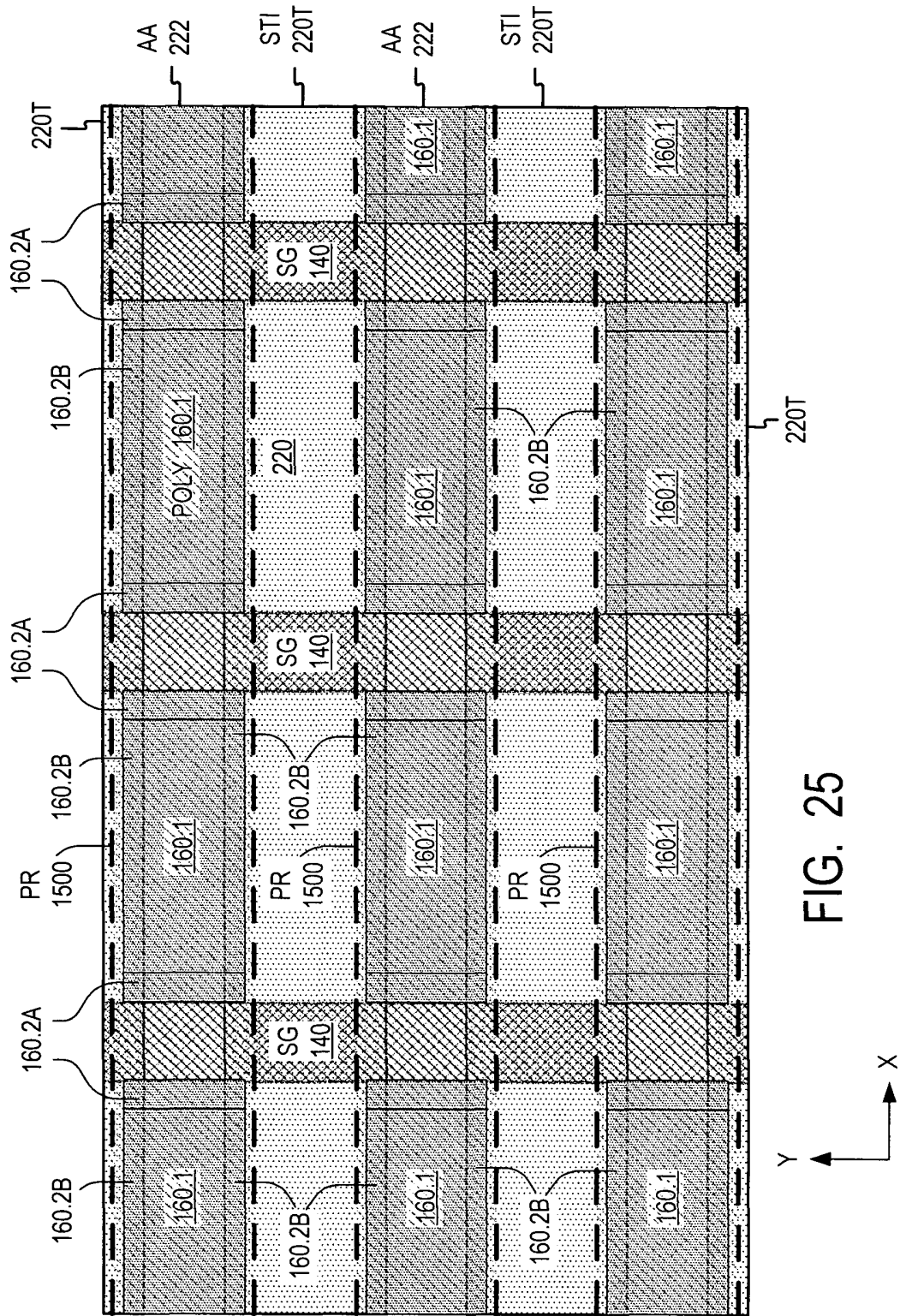


FIG. 25

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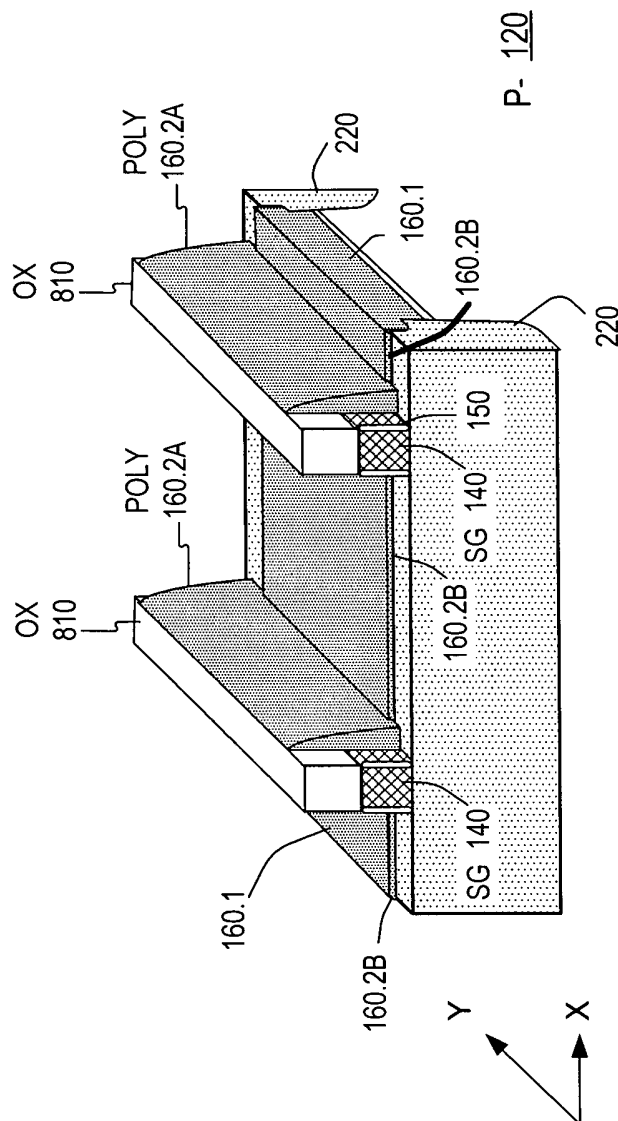


FIG. 26

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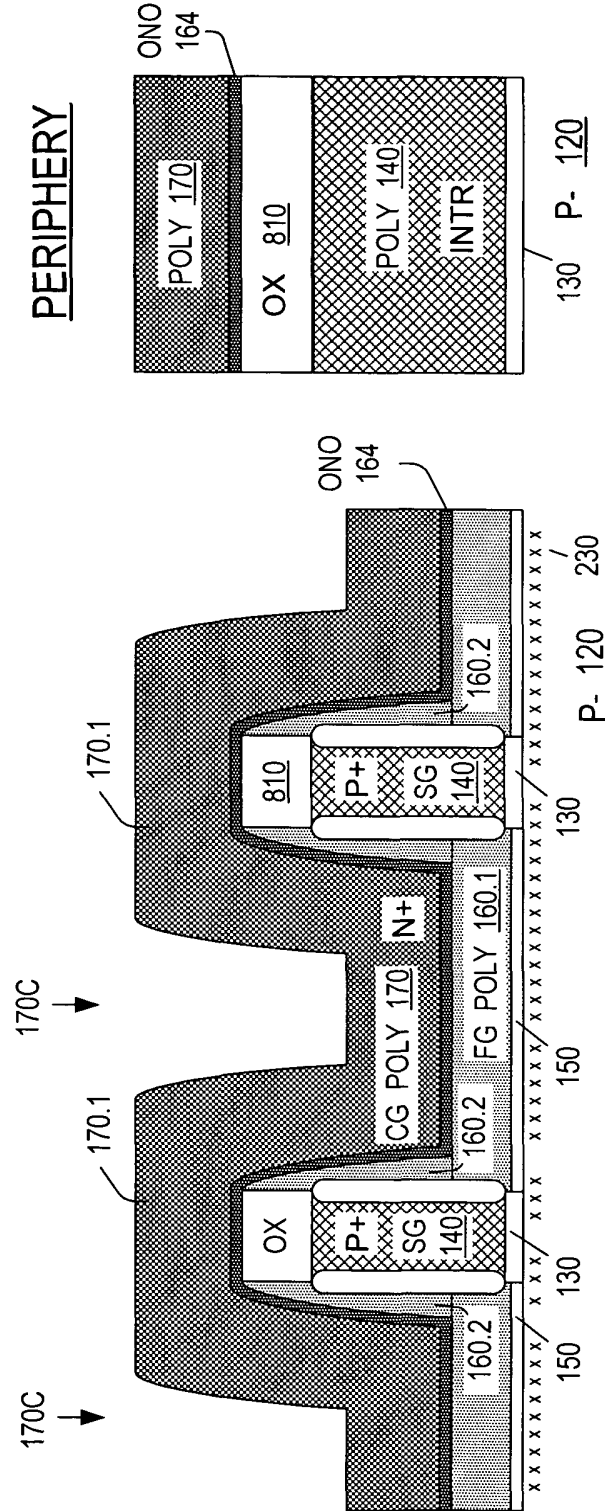


FIG. 27B

FIG. 27A (X1-X1'')

FIG. 28
(X1-X1')

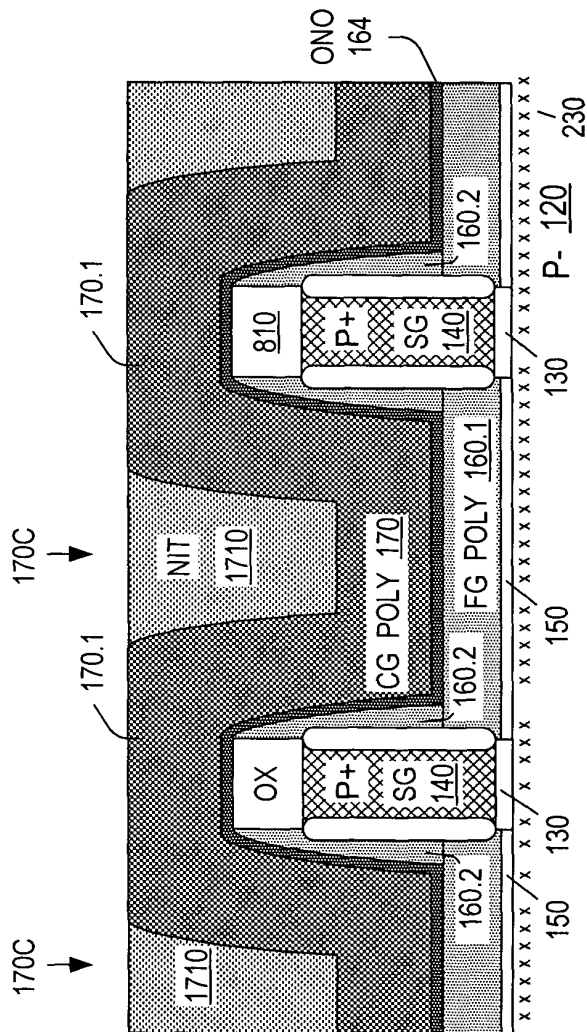


FIG. 29B

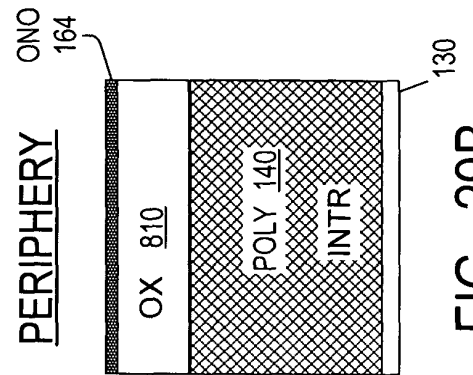


FIG. 29A (X1-X1')

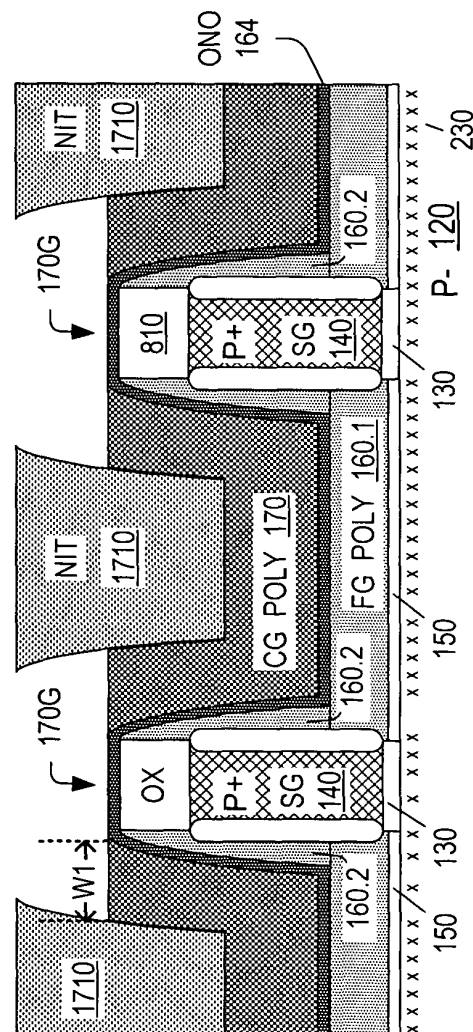


FIG. 30
(X1-X1')

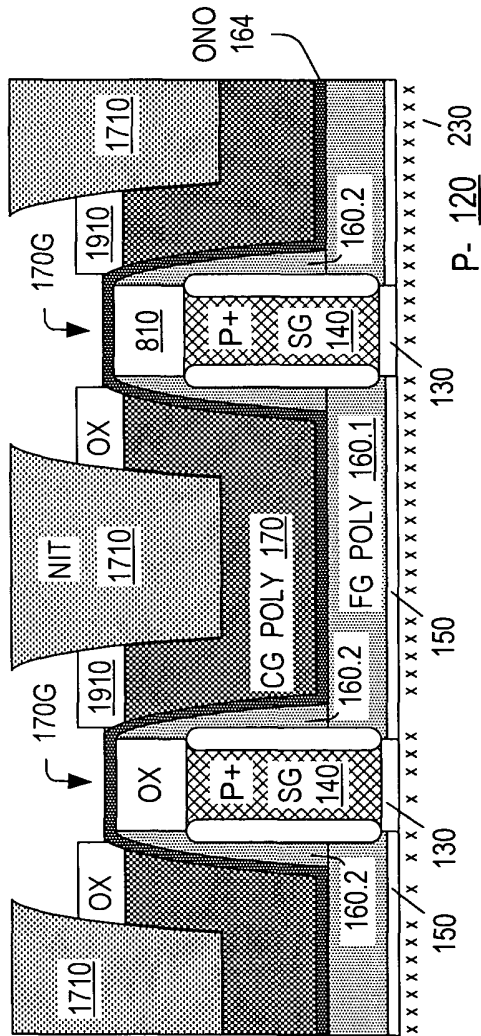
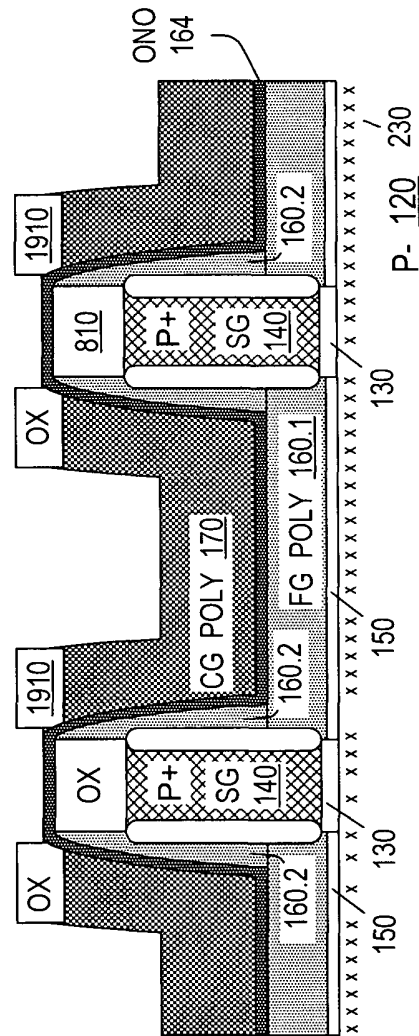


FIG. 31
(X1-X1')



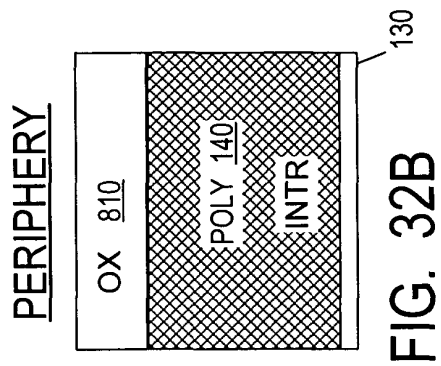
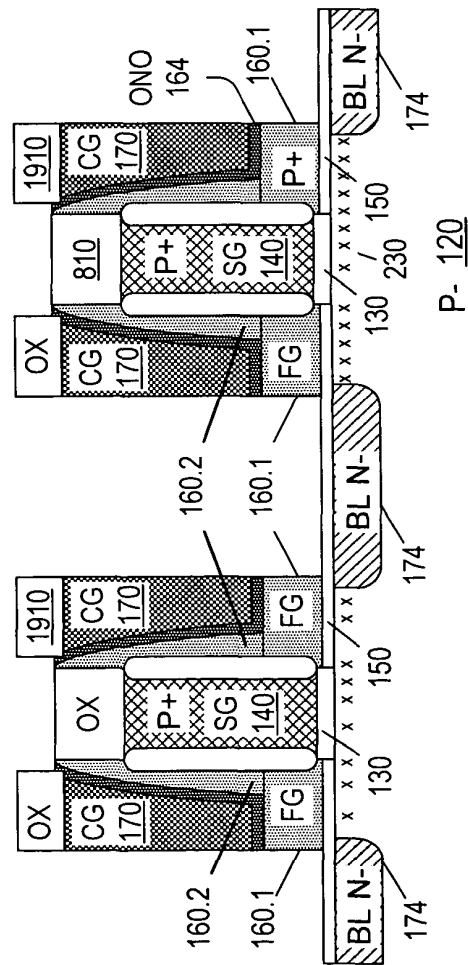
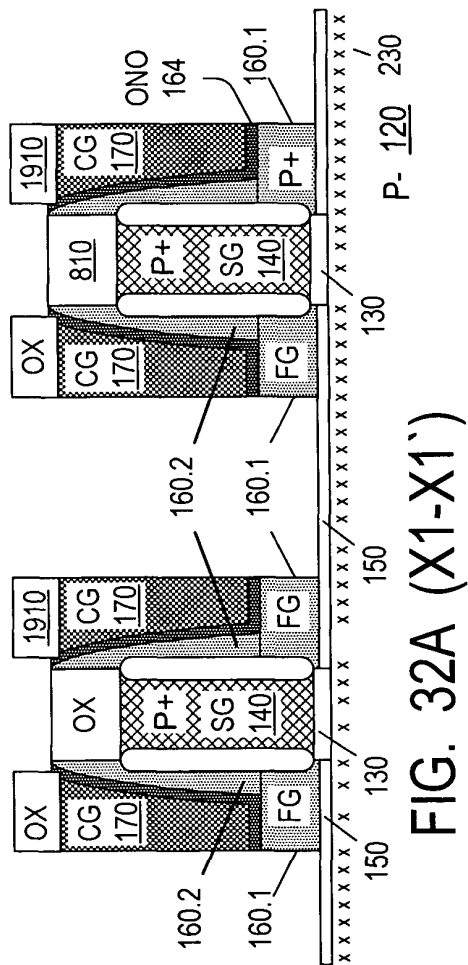


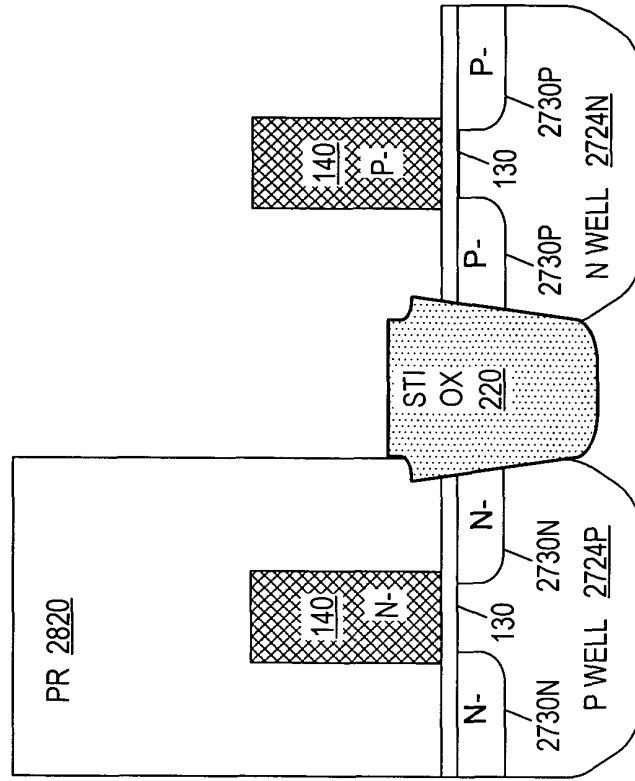
FIG. 33A
(X1-X1')



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PMOS 512P

NMOS 512N

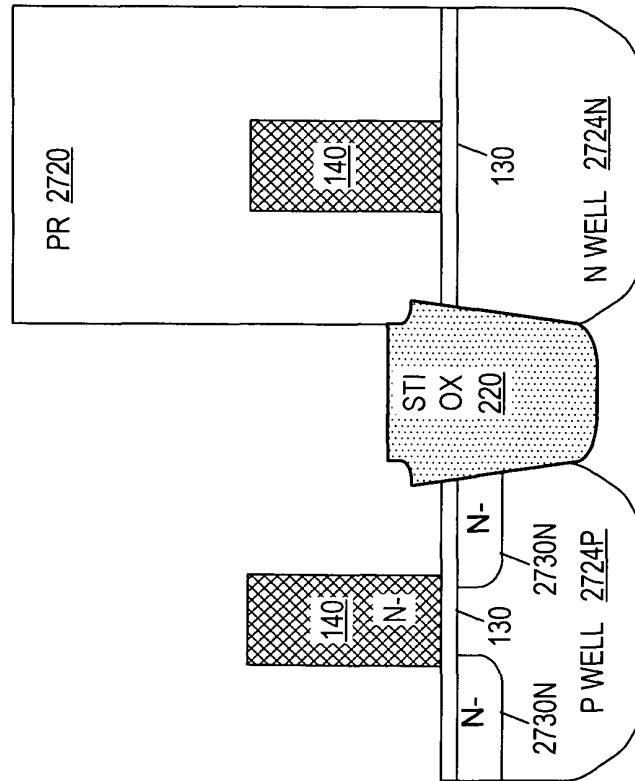


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FIG. 34
(PERIPHERY)

PMOS 512P

NMOS 512N



P- 120

FIG. 33B
(PERIPHERY)

FIG. 36A
(X1-X1')

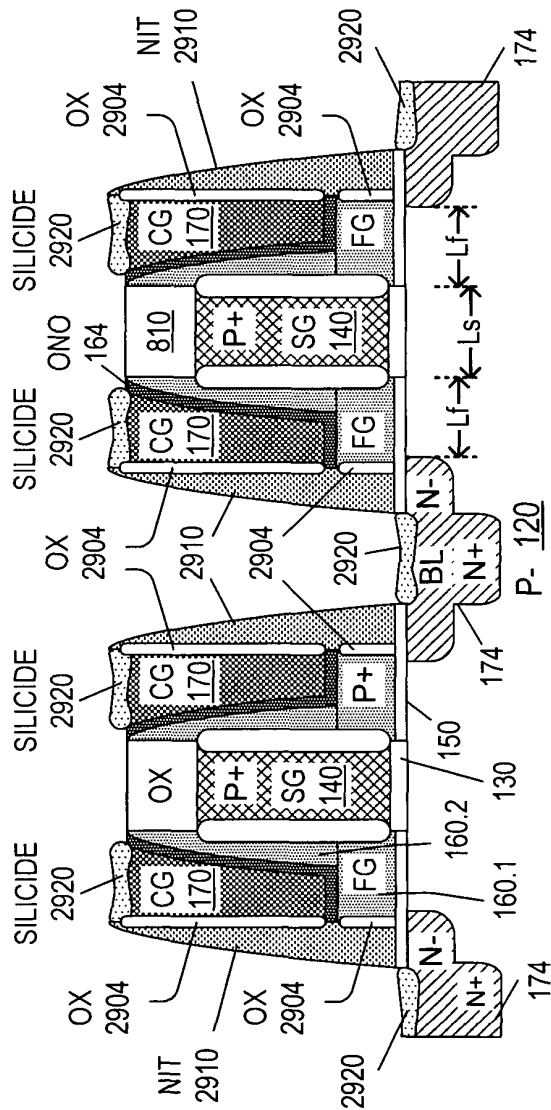
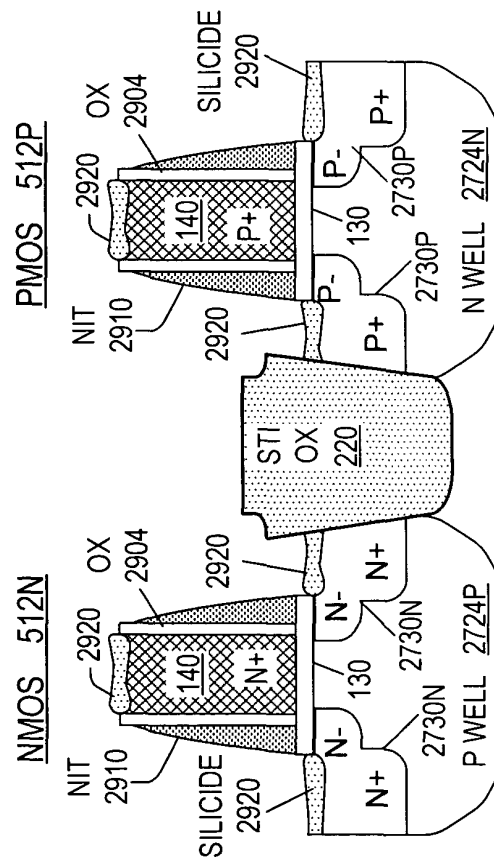


FIG. 36B
(PERIPHERY)



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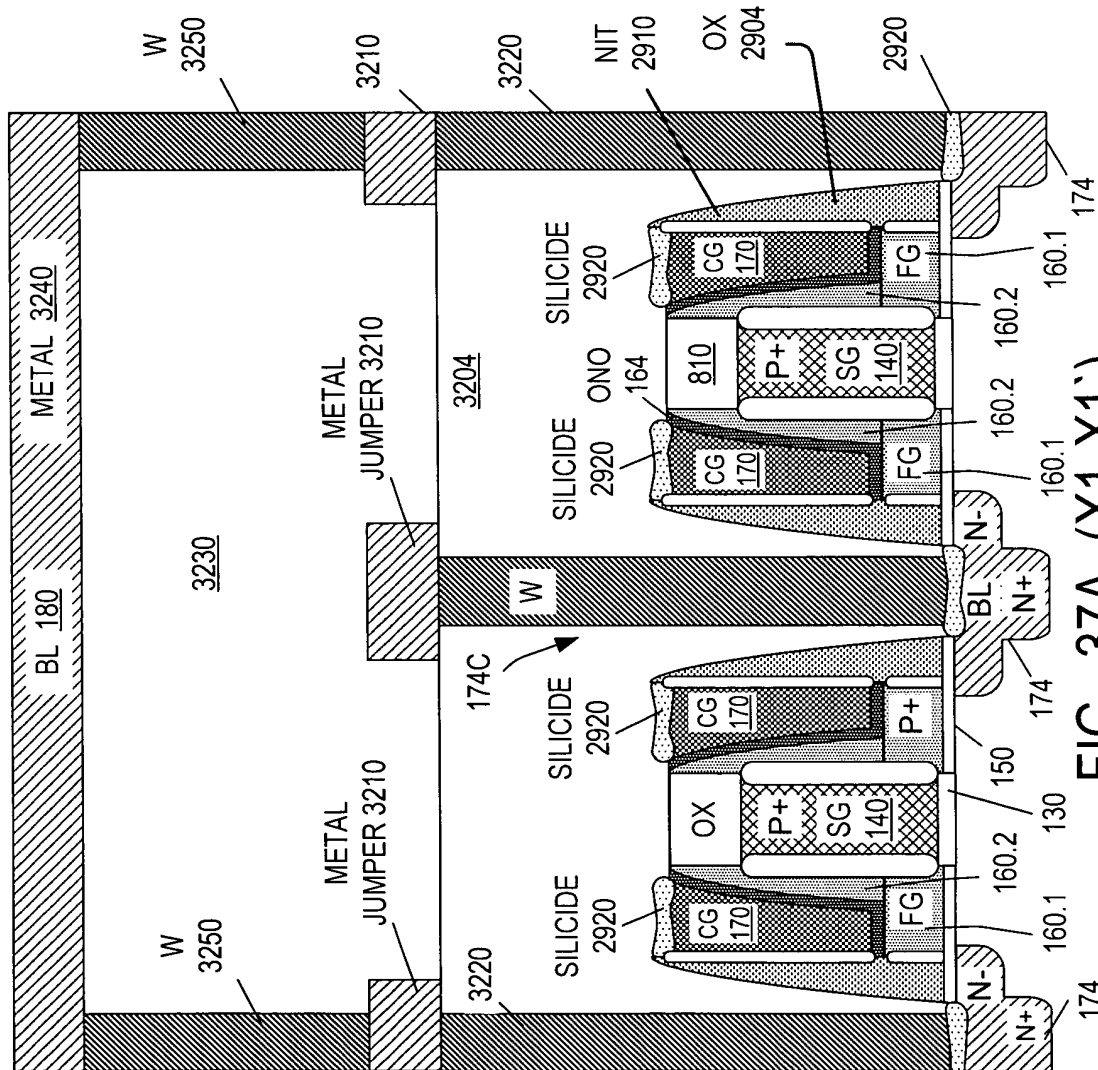


FIG. 37A (X1-X1')

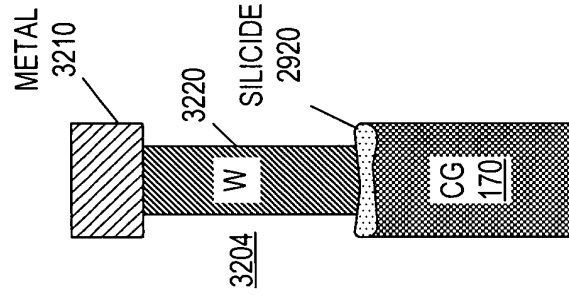


FIG. 37B
(ARRAY GAP OR
BOUNDARY)

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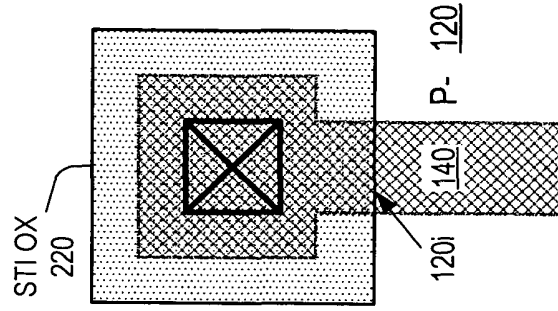


FIG. 37E
(PERIPHERY)

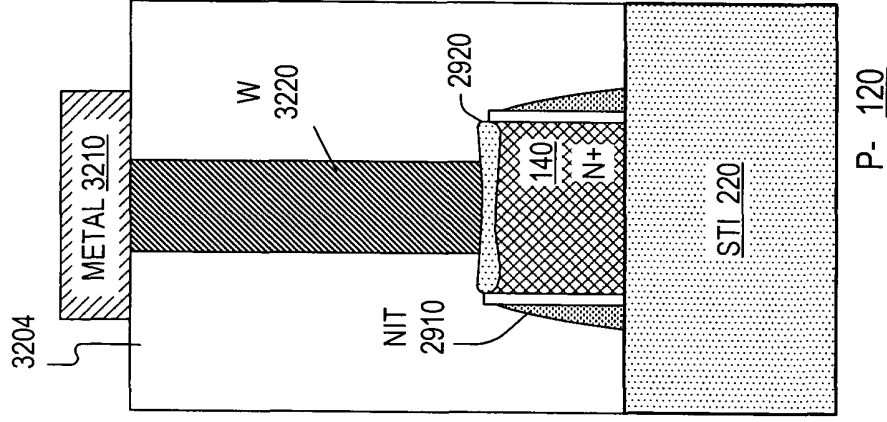


FIG. 37D
(PERIPHERY)

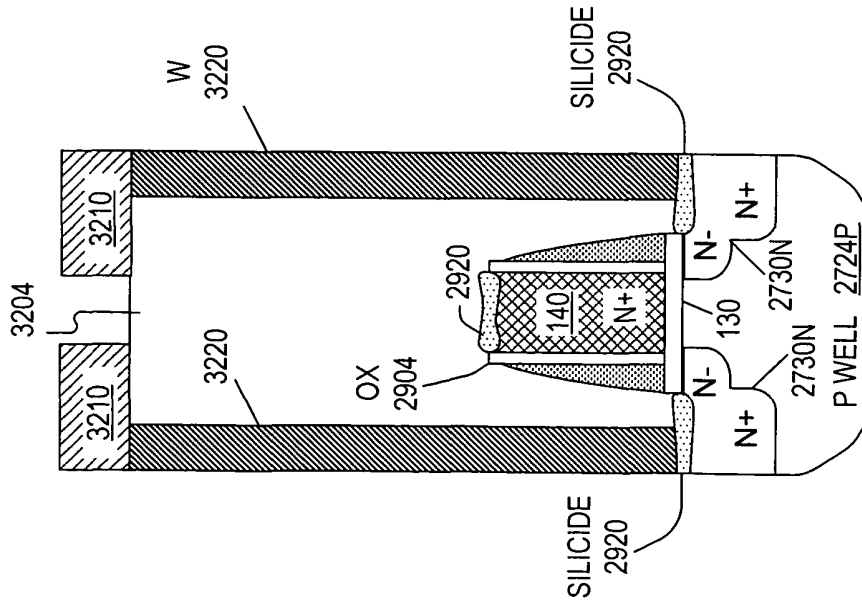


FIG. 37C
(PERIPHERY)

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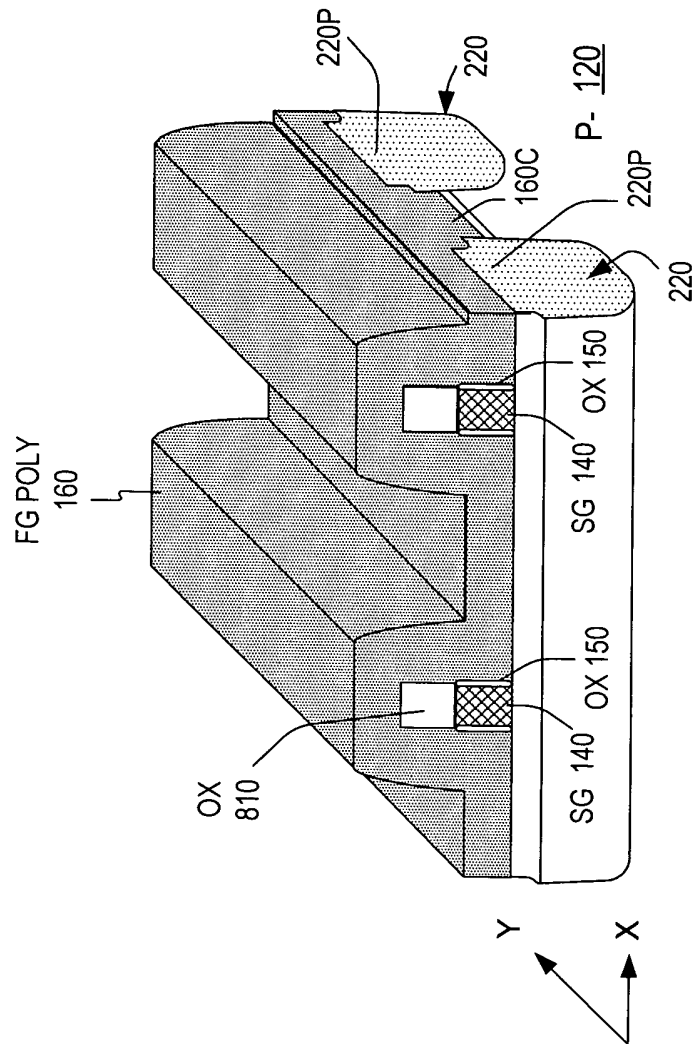


FIG. 38

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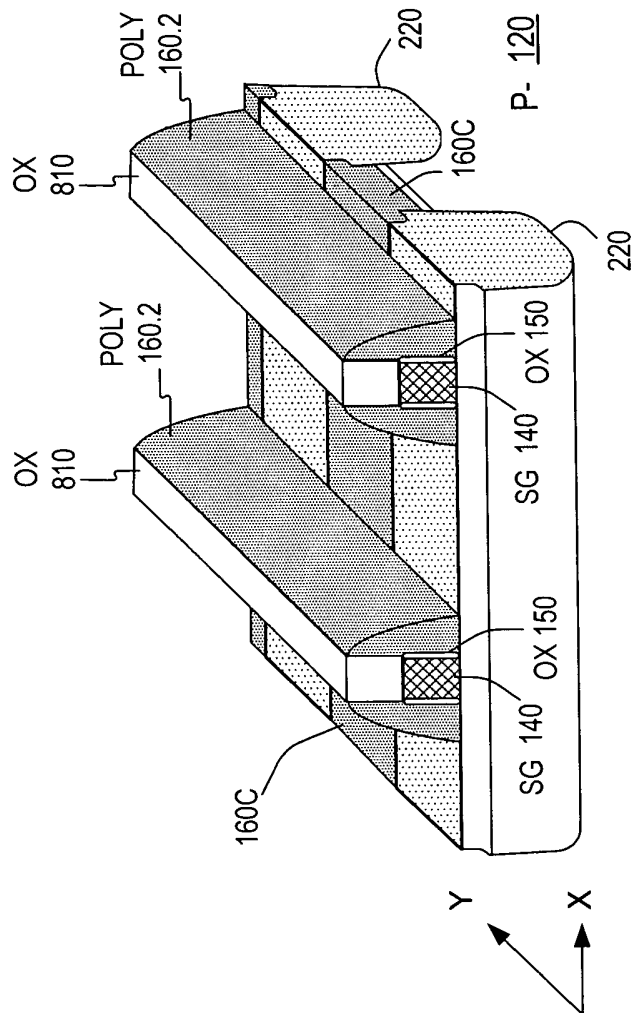


FIG. 39

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